

CMOS LATCHED COMPARATORS

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P R E F A C E

Nowadays due to the advancement of new technologies in the field of electronics, major importance is given towards the application with high speed and low power dissipation. Speed, low noise, and better slew rate, resolution are the important features of high speed applications such as sense amplifier, SOC design, data links etc.


In order to fulfil these specifications the basic building block i.e. comparator has to be tightly constrained. Hence design of comparator is more challenging one in the system.

From several decades many comparators are being used in many integrated circuits, but it is highly possible to modify or develop new topologies or expand known topologies of comparators for improving their performance.


This book presents new topologies of comparators in CMOS nanometer technologies. Numerous detailed circuit diagrams and plots of measured results allow a fast comprehension.

We wish to acknowledge our colleagues who contributed to this book with mind stimulating discussions. Thanks to the managements of Annamacharya Institute of Technology and Sciences(Autonomous), Rajampet and KL University for their financial support as well as the opportunity to use the design environment.

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