CMOS LATCHED COMPARATORS

Mr. N. Bala Dastagiri
Assistant Professor – ECE Dept.
Annamacharya Institute of Technology
Rajampet, Andhra Pradesh, INDIA.

Dr. K. Hari Kishore
Professor – ECE Dept.
KL University, Guntur, Andhra Pradesh, INDIA.

Dr. B. Abdul Rahim
Professor – ECE Dept.
Annamacharya Institute of Technology
Rajampet, Andhra Pradesh, INDIA.

Dr. S. Fahimuddin
Associate Professor – ECE Dept.
Annamacharya Institute of Technology
Rajampet, Andhra Pradesh, INDIA.

CMOS LATCHED COMPARATORS

ISBN-13: 978-93-86258-59-5
FIRST EDITION, JUNE 2017, INDIA

Typeset, Printed & Published by:
VSRD Academic Publishing
(*A Division of Visual Soft India Pvt. Ltd.*)

Printed & Bound in India

VSRD ACADEMIC PUBLISHING
A Division of Visual Soft India Pvt. Ltd.

REGISTERED OFFICE
154, Tezabmill Campus, Anwarganj, KANPUR–208003 (UP) (IN)
Mb: 99561 27040, Web: www.vsrdpublishing.com, Email: vsrdpublishing@gmail.com

MARKETING OFFICE (NORTH INDIA)
Basement-2, Villa-10, Block-V, Charmwood Village, FARIDABAD–121009 (HY)(IN)
Mb: 98999 36803, Web: www.vsrdpublishing.com, Email: vsrdpublishing@gmail.com

MARKETING OFFICE (SOUTH INDIA)
340, FF, Adarsh Nagar, Oshiwara, Andheri(W), MUMBAI–400053 (MH)(IN)
Mb: 99561 27040, Web: www.vsrdpublishing.com, Email: vsrdpublishing@gmail.com

PREFACE

Nowadays due to the advancement of new technologies in the field of electronics, major importance is given towards the application with high speed and low power dissipation. Speed, low noise, and better slew rate, resolution are the important features of high speed applications such as sense amplifier, SOC design, data links etc.

In order to fulfil these specifications the basic building block i.e. comparator has to be tightly constrained. Hence design of comparator is more challenging one in the system.

From several decades many comparators are being used in many integrated circuits, but it is highly possible to modify or develop new topologies or expand known topologies of comparators for improving their performance.

This book presents new topologies of comparators in CMOS nanometer technologies. Numerous detailed circuit diagrams and plots of measured results allow a fast comprehension.

We wish to acknowledge our colleagues who contributed to this book with mind stimulating discussions. Thanks to the managements of Annamacharya Institute of Technology and Sciences(Autonomous), Rajampet and KL University for their finanicial support as well as the opportunity to use the design environment.

Our family members deserve very special thanks for their continued support, encouragement and patience throughout this project.

✍ *N. Bala Dastagiri*

✍ *K. Hari Kishore*

✍ *B. Abdul Rahim*

✍ *Shaik Fahimuddin*

CONTENTS